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10/699,606	10/31/2003	Dominic Plunkett	093053.00001	9948

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EXAMINER	
NGUYEN, STEVE N	
ART UNIT	**PAPER NUMBER**
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

MN

Office Action Summary	Application No.	Applicant(s)	
	10/699,606	PLUNKETT, DOMINIC	
	Examiner	Art Unit	
	Steve Nguyen	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 23-25* is/are pending in the application.

4a) Of the above claim(s) *23-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 and 23-25 are currently pending.

Drawings

2. The amended drawings are accepted. The objection to the drawings in the first office action is withdrawn.

Claim Objections

3. In view of the amended claims, all objections in the prior Office Action are withdrawn. New objections are provided below.

Claim Rejections - 35 USC § 112

4. The U.S.C. 112, second paragraph rejection of claim 2 is maintained. Claim 2 recites, "whether the first pin is connected through the netlist to a second pin of a second device for which a BSDL file is present". It is unclear what is meant by a pin being "connected through the netlist" because a netlist is only an abstract representation of the connections in a circuit and does not physically make the connections.

Response to Arguments

5. Applicant's arguments filed 5/25/2007 have been fully considered but they are not persuasive.

The Applicant argues that Folea explicitly teaches away from including or using a net list, and it cannot be said that it would be obvious to refer to any other reference to include the feature which Folea explicitly seeks to avoid.

The examiner asserts that Folea does not seek to avoid using a netlist as alleged by Applicant. Folea explicitly states in col. 3, lines 11-14 that the tester does not replace the prior art, but rather augments it to provide users with a simple, manual method to control a boundary scan chain in real-time. In other words, Folea recognizes the necessity of the prior art methods of using a netlist for testing devices. The system of Folea is intended to provide those not having ordinary skill in the art (e.g. design engineers) with a simple way of running tests on boundary scan chains. However, anyone skilled in the art would have recognized that traditional methods would have been required for testing circuits without boundary-scan circuitry and therefore could not be completely replaced by the methods of Folea.

The Applicant argues that there is no suggestion in Lulla of providing separate BSDL files, a netlist and connections list and passing these three items to generate a data structure which, when combined with a test script, permits execution of the test script from the computer through the boundary scan bus.

The rejection in the Office action does not rely on providing separate BSDL files in Lulla, and so it is unclear why Applicant is arguing this point. The Examiner would

like to clarify that the rejection relies on using the method of Folea to test the circuit of Lulla. Lulla teaches a circuit 102 with JTAG support and a circuit 104 without JTAG support. A boundary-scan description language (BSDL) file would therefore be required for testing circuit 102, but not for circuit 104. Instead, a conventional netlist file would be required for testing circuit 104 since it is not a boundary-scan JTAG circuit. Furthermore, a netlist comprises a connection list as per the definition of "netlist" provided by the Authoritative Dictionary of IEEE Standards Terms, 7th Edition: *A point-to-point description of the interconnections between individual components in a circuit.*

The Applicant further argues that Lulla is not concerned with running test scripts, and accordingly there is no suggestion in Lulla of providing separate BSDL files, a netlist and connections list and passing these three items to generate a data structure which, when combined with a test script, permits execution of the test script from the computer through the boundary scan bus.

The Examiner would like to point out that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, Folea teaches running test scripts. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the test method of Folea for testing the circuit of Lully because the teachings of Folea do not require any special high-speed hardware and is extremely portable (col. 7, lines 35-40). In testing the circuit of Lully, a person skilled in the art would have recognized that a BSDL file would have been provided for

circuit 102 as per the description of Folea in col. 4, lines 56-58. However, a person skilled in the art would also have realized that the teachings of Folea would have to be modified to accept a netlist for the non-JTAG circuit 104 of Lully.

Claim Objections

6. Claim 2 objected to because of the following informalities:

- "for a the first pin" should be corrected to "for the first pin".
- in the recitation, "whereby the first, pin can be controlled", the comma should be removed.

Claim 8 objected to because "me second IC" should be "the second IC".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 2 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 2 recites, "The equipment of claim 1 for testing a first pin of a first device of the circuit to be tested, wherein the computer has all information necessary to identify whether, for the first pin, a BSDL file is present and whether the first pin is connected through the netlist to a second pin of a second device for which a BSDL file is present". The specification does not disclose that the first pin of a first device of the circuit to be tested has a BSDL file present. For example, pins 420-422 of first device to be tested 403 in Fig. 4 are not JTAG compatible. Therefore a BSDL file cannot be present because the device 403 is not a JTAG device. Similarly, Appendix 1 details a test example in which non-JTAG devices IC1, IC4, and IC5 are tested by JTAG capable IC2 and IC3. However, none of non-JTAG devices IC1, IC4, and IC5 being tested have a BSDL file present.

Election/Restrictions

8. Newly submitted claims 23-25 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: New claims 23-25 recite features substantially similar to non-elected claims 14 and 15 and are withdrawn from consideration for the same reasons.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 23-25 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1-13 rejected under 35 U.S.C. 103(a) as being unpatentable over Folea, Jr. (US Pat. 6,988,229; hereinafter referred to as Folea) in view of Lulla et al (US Pat. 6,757,844; hereinafter referred to as Lulla) in view of Tiong et al (US Pat. 6,539,520; hereinafter referred to as Tiong). Note: IEEE 1149.1 is brought in as a teaching reference in claims 5 and 13 to further show features of Folea, which adopts the standard.

As per claim 1:

Folea teaches circuit testing equipment comprising:

- a computer having stored thereon a boundary scan description language (BSDL) file (col. 4, lines 31-41); and

- a connector for connecting the computer to a boundary scan bus of a circuit to be tested (col. 3, lines 59-63);
- the computer being arranged to parse the BSDL file (col. 4, line 56) and generate a data structure therefrom which, when combined with a test script, permits execution of the test script from the computer through the boundary scan bus (col. 5, lines 7-19).

Not explicitly disclosed by Folea are a netlist and a connections list. However, Lulla teaches a device having at least one integrated circuit comprising a boundary-scan capable circuit that controls a circuit that is not boundary-scan capable (col. 2, lines 54-59). Tiong in an analogous art teaches a simplified method of creating BSDL and netlist files (col. 3, lines 26-31).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to test the apparatus of Lulla in the test system of Folea by using the system of Tiong to generate BSDL files of boundary-scan capable circuit 102 and netlist files of non-compliant JTAG circuit 104. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the system of Folea could test the circuit of Lulla without requiring special hardware (Folea; col. 7, lines 35-38) and that the method of Tiong simplifies the BSDL and netlist generation process (col. 3, lines 11-15).

As per claim 2:

Lulla further teaches the equipment of claim 1 for testing a first pin (Fig. 1,

element 122) of a first device of the circuit to be tested (Fig. 1, element 104), wherein the computer has all information necessary to identify whether, for the given pin, a BSDL file is present and whether the first pin is connected through the netlist to a second pin (Fig. 1, element 120) of a second device (Fig. 1, element 102) for which a BSDL file is present (col. 4, lines 35-41; complete BSDL information is provided in the system), whereby the first pin can be controlled using the boundary scan bus (col. 3, lines 21-24).

As per claim 3:

Folea further teaches the equipment according to claim 1, wherein the computer comprises a parser for parsing the BSDL file, the netlist and the connections, and a compiler for compiling the same to generate the data structure for execution with the test script (col. 4, lines 56-67).

As per claim 4:

Folea further teaches the equipment according to claim 1, wherein the computer further comprises at least one test script for testing an integrated circuit of the circuit to be tested (col. 5, lines 38-42).

As per claim 5:

Lulla further teaches the equipment according to claim 1, for testing a circuit that has at least one boundary-scan capable IC (col. 2, lines 55-56), the at least one boundary-scan capable IC having at least a first pin and a second pin (Fig. 1, elements 116 and 120), wherein at least the first pin is capable of adopting one of three states, being a high state, a low state and an input state (pin 120 is an input pin).

Not explicitly stated is the equipment further comprising connection test software arranged to test that the first and second pins are not connected, by setting the first pin to the input state and driving the second pin sequentially into the high and low states. However, IEEE 1149.1 teaches that the boundary scan register allows testing for short circuit connections between pins (page 60). Therefore, it would have been obvious to test the connection between two pins as suggested by IEEE 1149.1.

As per claim 6:

Folea further teaches the equipment according to claim 1, wherein the computer further comprises a first test script for testing a first integrated circuit of the circuit to be tested and a second test script for testing a second integrated circuit of the circuit to be tested (col. 5, lines 20-25; the system has a test script for any number of circuits).

As per claim 7:

Lulla further teaches the circuit testing equipment according to claim 1 for testing a circuit that has at least one first integrated circuit (IC) that is boundary-scan capable (col. 2, lines 55-56) and at least one second IC that is not boundary-scan capable (col. 2, lines 56-57), wherein the data structure defines all pins of the first IC that are capable of driving pins of the second IC (pins 116, 120, 124, 128, and 132 are driver pins; see Table 1) and all pins of the first IC that are capable of reading pins of the second IC (data is read through pin 120), whereby the second IC and its connections to the first IC can be tested by driving pins of the first IC (col. 1, lines 46-47).

As per claim 8:

Folea teaches circuit testing equipment for testing a circuit, the equipment comprising:

- an input for inputting files comprising a boundary scan description language (BSDL) file (col. 4, lines 31-41); and
- a data structure generated from the BSDL file (col. 5, lines 7-19),

Not explicitly disclosed by Folea is at least one first integrated circuit (IC) that is boundary-scan capable, and at least one second IC that is not boundary-scan capable; and netlist and connections list that defines all pins of the first IC that are capable of driving pins of the second IC and all pins of the first IC that are capable of reading pins of the second IC, whereby the second IC and its connections to the first IC can be tested by driving pins of the first IC.

However, Lulla teaches at least one first integrated circuit (IC) that is boundary-scan capable (col. 2, lines 55-56), and at least one second IC that is not boundary-scan capable (col. 2, lines 56-57); and pins of the first IC that are capable of driving pins of the second IC (pins 116, 120, 124, 128, and 132 are driver pins; see Table 1) and all pins of the first IC that are capable of reading pins of the second IC (data is read through pin 120), whereby the second IC and its connections to the first IC can be tested by driving pins of the first IC (col. 1, lines 46-47). Tiong in an analogous art teaches a simplified method of creating BSDL and netlist files (col. 3, lines 26-31).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to test the apparatus of Lulla in the test system of Folea by

using the system of Tiong to generate BSDL files of boundary-scan capable circuit 102 and netlist files of non-compliant JTAG circuit 104. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the system of Folea could test the circuit of Lulla without requiring special hardware (Folea; col. 7, lines 35-38) and that the method of Tiong simplifies the BSDL and netlist generation process (col. 3, lines 11-15).

Folea teaches initiating a test script for the boundary scan device under test in col. 5, lines, 38-42 to begin a scan operation. The test script is specific to the non-JTAG device under test because predefined controls for generating DUT-specific data can be selected by the user (col. 5, lines 49-54). The test script is independent of JTAG device 102 because connections between the devices are automatically mapped out and compensated for as shown by lines 510 in Fig. 5 of Lulla (col. 5, lines 28-32).

As per claim 9:

Lulla further teaches the equipment according to claim 7 wherein the first IC has pins that are capable of adopting one of three states, being a high state, a low state and an input state (pin 120 is an input pin).

As per claim 10:

Folea further teaches the equipment according to claim 7 wherein the first IC is connected to a boundary scan bus (Fig. 1, element 125).

As per claim 11:

Folea further teaches the equipment according to claim 7, further comprising a

parser and a compiler for parsing and compiling the BSDL file, the netlist and the connections list to generate the data structure, wherein the parser and compiler are implemented in computer programs loaded into a computer to be connected to the circuit to be tested (col. 4, lines 56-67).

As per claim 12:

Folea further teaches the equipment according to claim 11, wherein the computer further comprises a test script for testing the second IC and its connections to the first IC (col. 5, lines 29-41; a scan operation tests connections between circuits).

As per claim 13:

Lulla further teaches the equipment according to claim 8, wherein the at least one first IC has at least a first pin and a second pin (Fig. 1, elements 116 and 120), wherein at least the first pin is capable of adopting one of three states, being a high state, a low state and an input state (pin 120 is an input pin).

Not explicitly stated is the equipment further comprising connection test software arranged to test that the first and second pins are not connected, by setting the first pin to the input state and driving the second pin sequentially into the high and low states. However, IEEE 1149.1 teaches that the boundary scan register allows testing for short circuit connections between pins (page 60). Therefore, it would have been obvious to test the connection between two pins as suggested by IEEE 1149.1.

circuit to be tested.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steve Nguyen whose telephone number is (571) 272-7214. The examiner can normally be reached on M-F, 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Examiner
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